REMARKS

Claims 1-3, 5, 7, 8, 11, 12, 14, 19, 20, 24, 30 and 32-34 remain pending. By this Amendment, claims 14 and 30 are amended to address informalities.

The Office Action states a formality objection to specification page 3, line 15. However, the objection is not understood; the cited text appears to be clear. Also, what the Examiner suggests as a correction appears to be no different than the quoted present language. Should the objection be maintained, clarification thereof is respectfully requested. This is the second time that such clarification has been requested. See page 10 of the Amendment filed December 22, 2005.

The Office Action states formality objections regarding claims 14 and 30. Applicant has adopted the Examiner's suggested amendments to these claims to overcome the stated objections.

All of the pending claims stand rejected under 35 U.S.C. §103(a) as being unpatentable over Quayle et al. U.S. Patent No. 6,694,464 in view of the Kim et al. article. "A Reconfigurable Multi-Function Computing Cache Architecture," ACM 2000. This rejection is respectfully traversed.

As the Office Action acknowledges, the Quayle et al. patent does not disclose on-chip data processing resources used in the local generation and application of testing stimuli. Rather, Quayle et al. describe that code providing a behavioral test bench may be executed "in parallel on processors 206 of one or more of logic boards 200." Column 31, lines 64-67.

For the feature of on-chip testing, the Office Action now cites the Kim et al. article. However, the Office Action makes a number of assertions and characterizations which are incorrect concerning the disclosure of Kim et al., which apparently led to the erroneous

conclusion of obviousness. For example, with respect to clam 1, it is asserted that it would have been obvious to one of ordinary skill in the art "to modify the logic board of Quayle et al. with the logic board of Kim et al. that included at least one of the emulation ICs comprising on-chip programmable data processing resources to cooperate with and assist the on board data processing resources to perform the local generation and application of testing stimuli" Office Action, page 5. This assertion is specifically traversed.

Contrary to the Office Action assertion at page 5, the Kim et al. article does not disclose or suggest an emulation IC comprising on-chip programmable data processing resources to cooperate with and assist on-board data processing resources to perform the local generation and application of testing stimuli. The Kim et al. article is not concerned with, and does not disclose, a circuit emulation platform. Rather, the reconfigurable multi-function computing cache architecture disclosed by Kim et al. is for the purpose of providing a co-processor function unit from available cache memory on a microprocessor chip, to accelerate the execution of applications by the host microprocessor. In particular, the Kim et al. article describes the design of a reconfigurable module which works as both a function unit and as a cache memory. The function unit was designed to implement two computing primitives needed in structured video processing: FIR and DCT/IDCT. See Page 85, col. 2, par. 3.

At paragraph 8.2, concerning claim 3, the Office Action alleges "Kim et al. teaches that at least one of the emulation ICs comprises on-chip data processing resources to cooperate and assist the on-board data processing resources to perform the local monitoring and reporting of monitored events." This is incorrect because, as mentioned above, Kim et al. in fact do not even disclose an emulation platform or an emulation IC thereof, but rather disclose a microprocessor chip including a reconfigurable module which works as a function unit as well as a cache

memory. Kim et al. disclose nothing whatsoever concerning the testing/verification of a circuit design to be emulated on an emulation platform comprising one or more emulation integrated circuits.

Concerning claim 7, in section 8.3, at page 8, the Office Action alleges: "Kim et al. teaches that at least some of the generation of testing stimuli are performed by on-chip programmable data processing resources of the emulation ICs." This is incorrect, as explained above with regard to claim 1.

Concerning claim 8, Office Action section 8.4, page 9, states: "Kim et al. teaches that at least some of the analysis and detection are performed by on-chip data processing resources of the emulation ICs, in lieu of retrieving the state data from the emulation ICs." This is incorrect. As previously explained, Kim et al. in fact teach nothing regarding the testing of a circuit design emulated on an emulation IC.

Regarding claim 11, Office Action section 8.5, pages 9-10, states that "Kim et al. teaches that at least one of the emulation ICs comprises on-chip programmable data processing resources to cooperate with and assist the on-board data resources to perform the local generation and application of testing stimuli." This is incorrect, as mentioned above with regard to claim 1.

Regarding claim 14, Office Action section 8.6, at page 11, states that Kim et al. teaches that "at least some of the generation of testing stimuli are performed by on-chip programmable data processing resources of the emulation ICs." This is incorrect. Kim et al. neither discloses nor suggest anything of the sort. It could not be otherwise, given that Kim et al. disclose nothing about circuit emulation, much less the testing associated with verification of an emulated circuit design.

Regarding claim 19, Office Action section 8.7, page 12, alleges "Kim et al. teaches that at least one of the emulation ICs of the logic boards comprises on-chip programmable data processing resources to cooperate with and assist the on-board data processing resources of the logic board to perform the local and corresponding generation and application of testing stimuli." As explained above, Kim et al. in fact teach nothing concerning emulation ICs, much less the use of on-chip programmable data resources that cooperate with and assist on-board data processing resources to perform local generation and application of testing stimuli.

Regarding claim 23, Office Action section 8.8, at page 13, incorrectly states: "Kim et al. teaches that at least some of the performances of local and corresponding generation and application of testing stimuli are assisting by on-chip programmable data processing resources of the emulation ICs of the logic boards." Kim et al. in fact teach nothing of the sort, as explained above.

Regarding claim 30, section 8.9 of the Office Action, page 14, incorrectly states: "Kim et al. teaches locally retrieving on the emulation IC, using on-chip data processing resources, state data of emulated circuit elements of the emulation IC corresponding to a partition of an IC design being emulated; locally analyzing the state data of the emulation state circuit elements, using on-chip data processing resources; and locally generating testing stimuli using the on-chip programmable data processing resources; and locally applying the generated testing stimuli to an IC design being emulated, using the on-chip date processing resources." Kim et al. in fact teach nothing of the sort, as explained above.

Regarding claim 34, Office Action section 8.12, at page 16, incorrectly states "Kim et al. teaches the method of operation comprising locally generating on the emulation IC testing stimuli, using on-chip data processing resources; and locally applying the testing stimuli, using

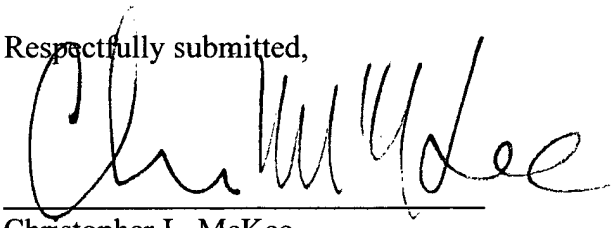
the on-chip data processing resources, to at least one of the emulation circuit elements." Kim et al. in fact teach nothing of the sort, as previously explained.

In sum, the Kim et al. article has been misconstrued to pertain to circuit emulation and more specifically to emulation ICs, when in fact it does not, but rather concerns the provision of a coprocessor on a microprocessor chip, in order to handle compute-intensive functions of applications run on the microprocessor. One of ordinary skill in the art would not have found it obvious to combine Qualye et al. and Kim et al. as proposed in the Office Action, given the very different objectives sought to be achieved by Quayle et al. on one hand, and Kim et al. on the other.

There is among the references no teaching or suggestion that Kim et al.'s reconfigurable multi-function computing cache architecture would have useful application in connection with the generation and application of testing stimuli on an emulation IC, so as to suggest a modification of Quayle et al. to include chip-level data processing resources as claimed. As noted above, the Kim et al. article in no way relates to the testing of an integrated circuit design being emulated on an emulation platform. Thus, the proposed combination lacks motivation and can be nothing more than an impermissible hindsight attempt to reconstruct the claimed invention given the benefit of Applicant's disclosure. Given that the asserted rejections are premised upon an incorrect interpretation of Kim et al. to pertain to the logical testing of circuitry emulated on an emulation platform, when in fact Kim et al. provide no such teaching whatsoever, the Office Action clearly fails to state a *prima facie* case of obviousness. Reconsideration and withdrawal of the rejections are respectfully requested.

For all of the foregoing reasons, it is respectfully submitted that this application is in condition for allowance. Should the Examiner believe that anything further is desirable in order to place the application in even better form for allowance, he is respectfully urged to telephone applicant's undersigned representative at the below-listed number.

Respectfully submitted,



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